This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-18. (Cancelled)

Claims 19-29. (Withdrawn)

~~1~~930. (Currently Amended) An assembly structure for a memory device, comprising:

a common substrate having multiple sections;

a first layer of a memory array disposed on a first section of the multiple sections wherein the first layer of the memory array comprises a first plurality of conductor lines;

a second layer of ~~a~~ the memory array disposed on a second section of the multiple sections wherein the second layer of the memory array comprises a second plurality of conductor lines;

at least one fold line disposed on the common substrate to define alignment of ~~the memory arrays on~~ the first and the second ~~sections~~ layers of the memory array;

~~wherein the sections may be folded on each other at the at least one fold line to form an operable electronic device in the memory device;~~

~~wherein at least one of the first and second layers of the memory array comprises semiconductor materials and patterns thereon to form a matrix of memory cells~~; and

a layer of semiconductor materials disposed on at least one of the first and the second layers the memory array,

wherein the first and second sections are configured to be folded along the at least one fold line so that the first and the second layers of the memory array are in contact with each other and wherein the first and the second plurality of conductor lines are arranged to interact with each other and the layer of semiconductor materials upon folding to form at least one memory cell spanning the first and the second layers of the memory array at intersections of the first and the second plurality of conductor lines.

~~20~~31. (Previously Presented) The assembly structure recited in claim ~~19~~30, wherein the first plurality of conductor lines are fabricated with first narrowing cross-sections areas at points where the memory cells are capable of a permanent change of state.

~~21~~32. (Previously Presented) The assembly structure recited in claim ~~20~~31, wherein the second plurality of conductor lines includes a second narrowing cross-section areas configured to align with the first narrowing cross-sections areas.

33. (New) The assembly structure recited in claim 30, wherein the memory cell comprises a diode and a fuse in series.

34. (New) An assembly structure for a memory device, comprising:

a common substrate having multiple sections;

a first layer of a memory array disposed on a first section of the multiple sections wherein the first layer of the memory array comprises a first plurality of conductor lines;

a second layer of the memory array disposed on a second section of the multiple sections wherein the second layer of the memory array comprises a second plurality of conductor lines;

at least one fold line disposed on the common substrate to define alignment of the memory arrays on the first and the second sections;

wherein the first plurality of conductor lines are fabricated with first narrowing cross-sections areas at points where the memory cells are capable of a permanent change of state;

wherein the sections may be folded on each other at the at least one fold line to form an operable electronic device in the memory device;

wherein at least one of the first and the second layers of the memory array comprises semiconductor materials and patterns thereon to form a matrix of memory cells; and

wherein the first and the second sections are folded along the at least one fold line so that the layers of the memory array are in contact with each other.

35. (New) The assembly structure recited in claim 34, wherein the second plurality of conductor lines includes a second narrowing cross-section areas configured to align with the first narrowing cross-sections areas.